IN THE CLAIMS:

The status of the claims is as follows.

1. (canceled)

2. (currently amended) ~~The device according to claim 1~~ A high speed interface type semiconductor memory device, comprising:

a controller constructed and arranged to transmit a clock signal and data signals synchronized with the clock signal to a plurality of DRAMs, and receive data signals from the DRAMs; and

a DRAM module unit constructed and arranged to generate a strobe clock signal for synchronizing a data signal during a read operation in the DRAM farthest from the controller among the plurality of DRAMs, provide the strobe clock signal to the other DRAMs, and transmit data to the controller during the read operation,

wherein each DRAM comprises:

a first buffer constructed and arranged to receive main clock and clock bar signals from the controller;

a second buffer constructed and arranged to buffer a first internal clock signal obtained by delay locking the main clock signal according to a control signal, and output data strobe clock and clock bar signals;

a third buffer constructed and arranged to buffer and output the data strobe clock and clock bar signals according to the control signal;

a DLL unit constructed and arranged to receive the output signal from the first buffer and the output signal from the third buffer, and output the first internal clock and clock bar signals, second internal clock and clock bar signals obtained by 90° phase-shifting the first internal clock and clock bar signals, third internal clock and clock bar signals, and fourth internal clock and clock bar signals obtained by 90° phase-shifting the third internal clock and clock bar signals;

a first multiplexer unit constructed and arranged to selectively transmit the first internal clock and clock bar signals or the third internal clock and clock bar signals according to the control signal;

a second multiplexer unit constructed and arranged to selectively transmit the second internal clock and clock bar signals or the fourth internal clock and clock bar signals according to the control signal;

a read first-in first-out unit constructed and arranged to synchronize and output a 4 bit read data according to the output signals from the first and second multiplexer units;

a fourth buffer connected between the read first-in first-out unit and a DQ pad;

a fifth buffer constructed and arranged to receive a write data inputted through the DQ pad; and

a write first-in first-out unit constructed and arranged to receive the output signal from the fifth buffer, synchronize the output signal according to the first internal clock and clock bar signals and the second internal clock and clock bar signals, and output a 4 bit write data.

3. (currently amended) The device according to claim 2 [[1]], wherein the first internal clock and clock bar signals and the third internal clock and clock bar signals are delay locked signals by the DLL unit receiving the main clock and clock bar signals.